# 2N7002L

# Small Signal MOSFET

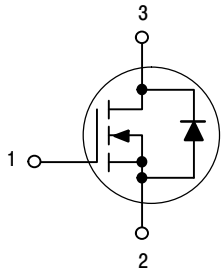
## 60 V, 115 mA, N–Channel SOT–23

**ON Semiconductor®**

**http://onsemi.com**

| $V_{(BR)DSS}$ | $R_{DS(on)}$ MAX | $I_D$ MAX |
|---|---|---|
| 60 V | 7.5 Ω @ 10 V, 500 mA | 115 mA |

**N–Channel**




### Features

- AEC Qualified
- PPAP Capable
- Pb–Free Packages are Available

### MAXIMUM RATINGS

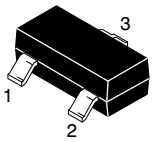
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Drain Current<br>– Continuous $T_C$ = 25°C (Note 1)<br>$T_C$ = 100°C (Note 1)<br>– Pulsed (Note 2) | $I_D$<br>$I_D$<br>$I_{DM}$ | ±115<br>±75<br>±800 | mAdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \le 50$ μs) | $V_{GS}$<br>$V_{GSM}$ | ±20<br>±40 | Vdc<br>Vpk |

### THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Total Device Dissipation FR–5 Board (Note 3) $T_A$ = 25°C<br>Derate above 25°C | $P_D$ | 225<br>1.8 | mW<br>mW/°C |
| Thermal Resistance, Junction–to–Ambient | $R_{\theta JA}$ | 556 | °C/W |
| Total Device Dissipation Alumina Substrate,(Note 4) $T_A$ = 25°C<br>Derate above 25°C | $P_D$ | 300<br>2.4 | mW<br>mW/°C |
| Thermal Resistance, Junction–to–Ambient | $R_{\theta JA}$ | 417 | °C/W |
| Junction and Storage Temperature | $T_J$, $T_{stg}$ | –55 to +150 | °C |

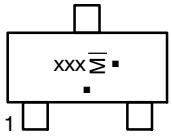
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The Power Dissipation of the package may result in a lower continuous drain current.
2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
3. FR–5 = 1.0 x 0.75 x 0.062 in.
4. Alumina = 0.4 x 0.3 x 0.025 in 99.5% alumina.




**SOT–23**
**CASE 318**
**STYLE 21**

**MARKING DIAGRAM**




702 = Device Code
M = Date Code*
▪ = Pb–Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| 2N7002LT1 | SOT–23 | 3000 Tape & Reel |
| 2N7002LT3 | | 10,000 Tape & Reel |
| 2N7002LT1G | SOT–23 (Pb–free) | 3000 Tape & Reel |
| 2N7002LT3G | | 10,000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain−Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 10 μAdc) | | $V_{(BR)DSS}$ | 60 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{GS}$ = 0, $V_{DS}$ = 60 Vdc) | $T_J$ = 25°C<br>$T_J$ = 125°C | $I_{DSS}$ | –<br>– | –<br>– | 1.0<br>500 | μAdc |
| Gate−Body Leakage Current, Forward ($V_{GS}$ = 20 Vdc) | | $I_{GSSF}$ | – | – | 100 | nAdc |
| Gate−Body Leakage Current, Reverse ($V_{GS}$ = −20 Vdc) | | $I_{GSSR}$ | – | – | −100 | nAdc |
| **ON CHARACTERISTICS** (Note 5) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | – | 2.5 | Vdc |
| On−State Drain Current ($V_{DS}$ ≥ 2.0 $V_{DS(on)}$, $V_{GS}$ = 10 Vdc) | | $I_{D(on)}$ | 500 | – | – | mA |
| Static Drain−Source On−State Voltage<br>($V_{GS}$ = 10 Vdc, $I_D$ = 500 mAdc)<br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 50 mAdc) | | $V_{DS(on)}$ | <br>–<br>– | <br>–<br>– | <br>3.75<br>0.375 | Vdc |
| Static Drain−Source On−State Resistance<br>($V_{GS}$ = 10 V, $I_D$ = 500 mAdc)<br><br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 50 mAdc) | <br>$T_C$ = 25°C<br>$T_C$ = 125°C<br>$T_C$ = 25°C<br>$T_C$ = 125°C | $r_{DS(on)}$ | <br>–<br>–<br>–<br>– | <br>–<br>–<br>–<br>– | <br>7.5<br>13.5<br>7.5<br>13.5 | Ohms |
| Forward Transconductance ($V_{DS}$ ≥ 2.0 $V_{DS(on)}$, $I_D$ = 200 mAdc) | | $g_{FS}$ | 80 | – | – | mmhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | | $C_{iss}$ | – | – | 50 | pF |
| Output Capacitance ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | | $C_{oss}$ | – | – | 25 | pF |
| Reverse Transfer Capacitance ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | | $C_{rss}$ | – | – | 5.0 | pF |
| **SWITCHING CHARACTERISTICS** (Note 5) | | | | | | |
| Turn−On Delay Time | ($V_{DD}$ = 25 Vdc, $I_D$ ≅ 500 mAdc, $R_G$ = 25 Ω, $R_L$ = 50 Ω, $V_{gen}$ = 10 V) | $t_{d(on)}$ | – | – | 20 | ns |
| Turn−Off Delay Time | | $t_{d(off)}$ | – | – | 40 | ns |
| **BODY−DRAIN DIODE RATINGS** | | | | | | |
| Diode Forward On−Voltage ($I_S$ = 11.5 mAdc, $V_{GS}$ = 0 V) | | $V_{SD}$ | – | – | −1.5 | Vdc |
| Source Current Continuous (Body Diode) | | $I_S$ | – | – | −115 | mAdc |
| Source Current Pulsed | | $I_{SM}$ | – | – | −800 | mAdc |

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

## TYPICAL ELECTRICAL CHARACTERISTICS

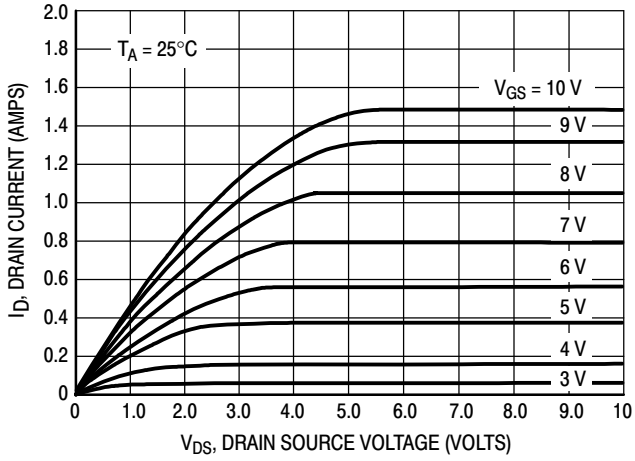



**Figure 1. Ohmic Region**

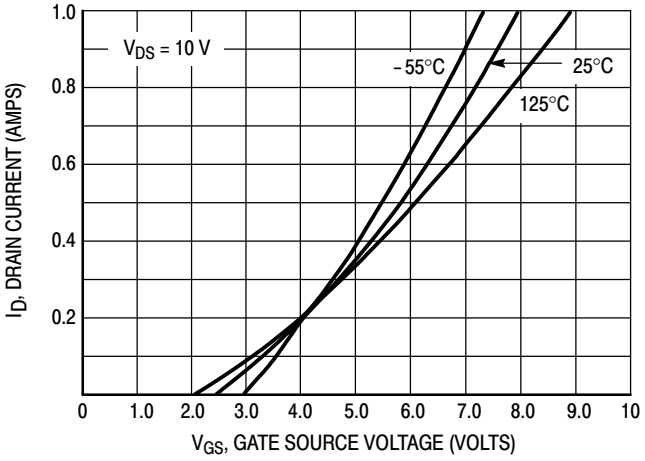



**Figure 2. Transfer Characteristics**

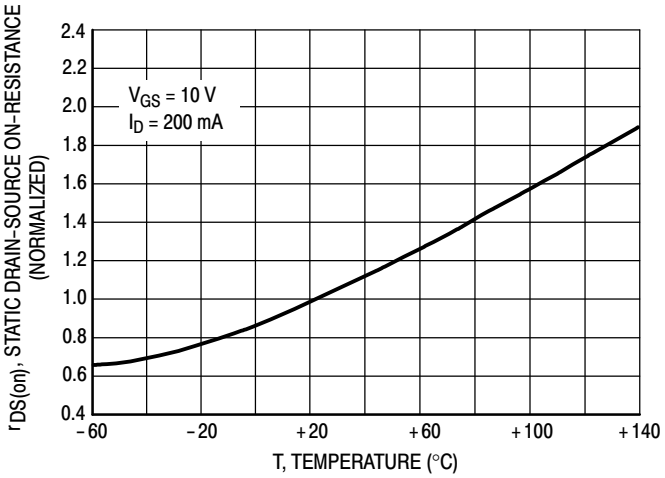



**Figure 3. Temperature versus Static Drain−Source On−Resistance**

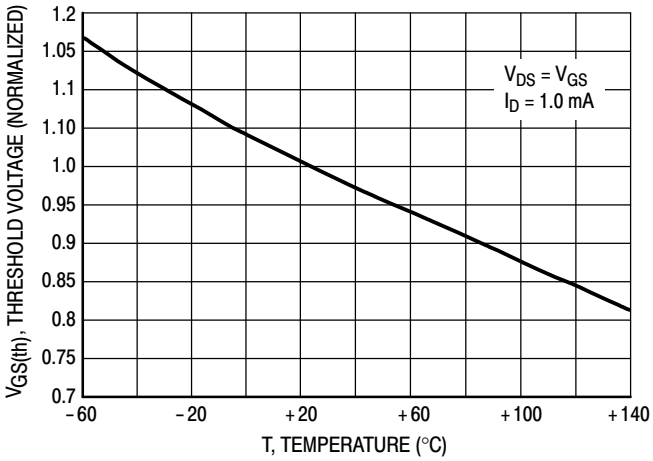
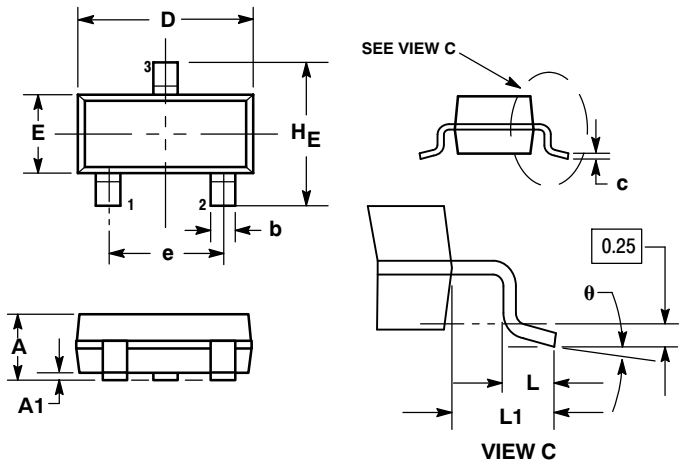



**Figure 4. Temperature versus Gate Threshold Voltage**

## PACKAGE DIMENSIONS

**SOT−23 (TO−236)**
CASE 318−08
ISSUE AN

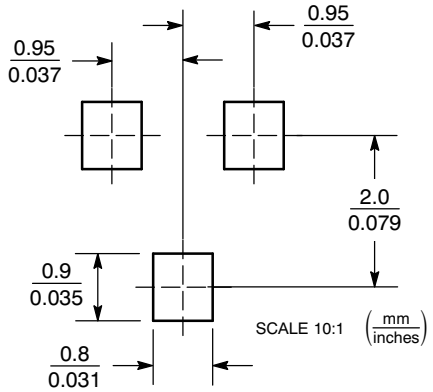



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−01 THRU −07 AND −09 OBSOLETE, NEW STANDARD 318−08.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.89 | 1.00 | 1.11 | 0.035 | 0.040 | 0.044 |
| A1 | 0.01 | 0.06 | 0.10 | 0.001 | 0.002 | 0.004 |
| b | 0.37 | 0.44 | 0.50 | 0.015 | 0.018 | 0.020 |
| c | 0.09 | 0.13 | 0.18 | 0.003 | 0.005 | 0.007 |
| D | 2.80 | 2.90 | 3.04 | 0.110 | 0.114 | 0.120 |
| E | 1.20 | 1.30 | 1.40 | 0.047 | 0.051 | 0.055 |
| e | 1.78 | 1.90 | 2.04 | 0.070 | 0.075 | 0.081 |
| L | 0.10 | 0.20 | 0.30 | 0.004 | 0.008 | 0.012 |
| L1 | 0.35 | 0.54 | 0.69 | 0.014 | 0.021 | 0.029 |
| $H_E$ | 2.10 | 2.40 | 2.64 | 0.083 | 0.094 | 0.104 |

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

## SOLDERING FOOTPRINT




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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